# WQ9001

## Data Sheet

**Release V1.1**

目录

# Revision History

| Publication Date | Version | Edition |
|---|---|---|
| October 2021 | V1.0 | First Edition |
| | | |

# 1. Overview

interface and power management circuits. The integrated RF circuits include power amplifier (PA), WQ9001 is a highly integrated, high performance 802.11 b/g/n WLAN SoC chip with USB interface (USB 2.0 compliant). WQ9001 integrates RF transceiver, 802.11 PHY & MAC, RISC-V CPU, OTP, USB low noise amplifier (LNA), T/R switch and balun. Therefore, WQ9001 provides a complete solution for high throughput and reliable wireless LAN application.

WQ9001 supports all data rates for IEEE 802.11 b/g/n with one spatial stream transmission over 20MHz bandwidth.

## 1.1 Application

- IP camara
- TV
- Set-top box
- PC

## 1.2 Features

- General
  - Integrated RF transceiver, 802.11 PHY & MAC, RISC-V CPU, OTP, USB interface and power management circuits in a single chip
  - Integrated PA, LNA, T/R switch and balunto minimize BOM cost
  - Integrated LDO'son chip, only 3.3v power is needed
  - Support AP & STA function
  - 40MHz crystal
  - RISC-V CPU with speedup to 160MHz
  - 1k bits OTP
  - 224KB on-chip SRAM
  - 128KB on-chip ROM
- Standards Supported
  - IEEE 802.11 b/g/n
  - IEEE 802.11 e(WMM)

    Encryption: open / WEP40 / WEP104 / TKIP / AES128 in STA mode, open / AES128 in AP mode

- Authentication: WEP share-key / WPA / WPA2 in STA mode, WAP2 in AP mode

- WLAN MAC Features
  - Up to 8 aggregation streams Tx AMPDU
  - Up to 8 aggregation streams Rx AMPDU
  - Rx BA scoreboard
  - Immediate-BA
  - Power saving mod

- WLAN PHY Features
  - One transmission and one receive path (1T1R)
  - Compatible with 802.11n legacy mode and mix mo e
  - Supports 20MHz bandwidth transmission
  - Maximum data rate: 54Mbps in 802.11g and 72Mb s in 802.11n
  - Supports STBC reception
  - Supports short-GI (Guard Interval)
  - Supports fast AGC (Automatic Gain Control
  - Supports self-calibration for IQ-m smatc an DC offset
  - Supports digital pre-distortion

- Peripheral Interfaces
  - 7 *GPIO(3.3V
  - 1 * watchdog
  - 4 * GP timer
  - USB interface with speedup to 480Mbps (complies with USB 2.0)
  - 1 * High speed UART

- Package
  - 4x4 $mm^2$, 24-pin QFN package

# 2. Functional Block Diagram

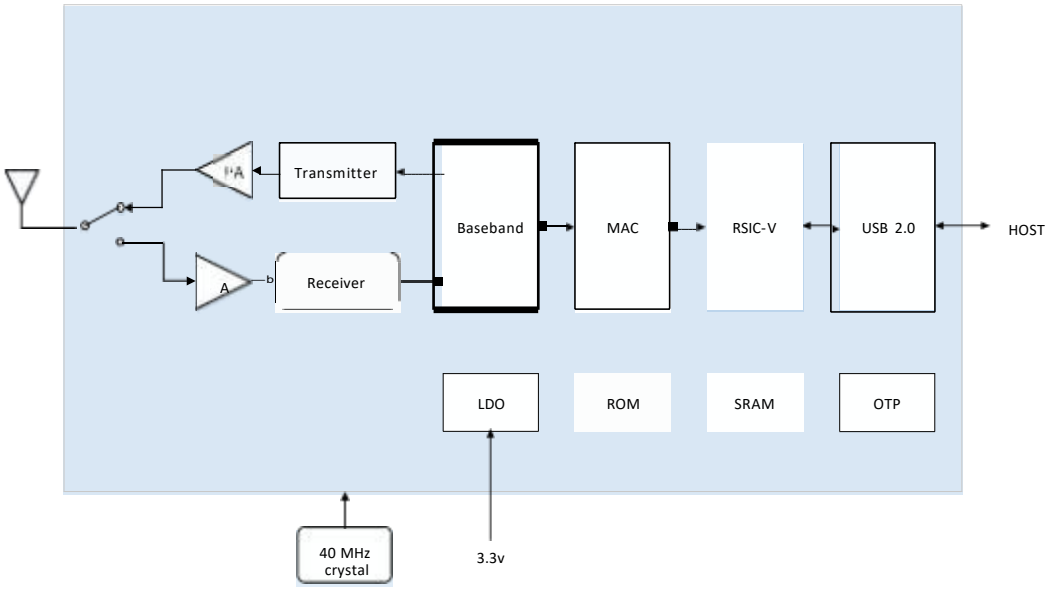


**Figure 2-1 Functional Block Diagram**

## 2.1.1 System Boot/Reset

- WQ9001 integrate one POR (Power on Reset) block, once the power satisfy the power-on requirement (VDD33> 2.7 V), power-on sequence will be generated by hardware to boot the chip.
- WQ9001 inte rate BOR (Brown-out Reset) circuit, once VDD33 is smaller than 2.6V, the chip will be reset

# 3. Pin Descriptions

This section contains both a package pinout and tabular listings of the signal descriptions.

The following nomenclature is used for Signal types:

| | |
|---|---|
| GND | A Ground Signal |
| IA | Analog input signal |
| I | Digital input signal |
| IH | Input signals with weak internal pull-up, to prevent signals from floating when left open |
| IL | Input signals with weak internal pull-down, to prevent signals from floating when left open |
| I/O | A digital bi-directional signal |
| OA | An analog output signal |
| O | A digital output signal |
| P | A power or ground signal |

## 3.1 Pin Assignments

The WQ9001 package is a Pb-free 4mmx 4mm 24- in QFN.

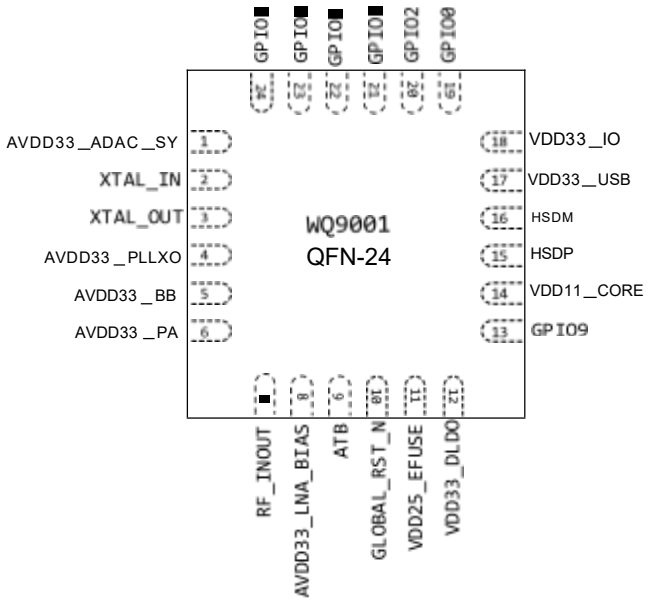


**Figure 3-2 WQ9001 4 mmx 4 mm 24-Pin QFN**

## 3.2 Signal-to-Pin Relationships and Descriptions

Table 3-1 provides the signal-to-pin number relationship information for the WQ9001.

**Table 3-1 Pin Assignments**

| No. | Name | Type | Power | Description |
|---|---|---|---|---|
| 1 | AVDD33_ADAC_SYN | P | 3.3V | VDD 3.3v for ADC, DAC and SYN |
| 2 | XTAL_IN | I | | Input of 40MHz crystal clock reference |
| 3 | XTAL_OUT | O | | Output of 40MHz crystal clock reference |
| 4 | AVDD33_PLLXO | P | 3.3V | VDD 3.3v for PLL, XO |
| 5 | AVDD33_BB | P | 3.3V | VDD 3.3v for BB |
| 6 | AVDD33_PA | P | 3.3V | VDD 3.3v for PA |
| 7 | RF_INOUT | I/O | | RF TRX signal |
| 8 | AVDD33_LNA_BIAS | P | 3.3V | VDD 3.3v for LNA BIAS |
| 9 | ATB | O | | Analog test pin |
| 10 | GLOBAL_RST_N | I | | Global reset (active low) |
| 11 | VDD25_EFUSE | P | 3.3V | VDD 2.5v for EFUSE |
| 12 | VDD33_DLDO | P | 3.3V | VDD 3.3v for digital LDO |
| 13 | GPIO9 | I/O | | GPIO9 |
| 14 | VDD11_CORE | P | 1.1V | VDD 1.1v for digital core |
| 15 | HSDP | I/O | | USB transceiver differential pair |
| 16 | HSDM | I/O | | USB transceiver differential pair |
| 17 | VDD33_USB | P | 3.3V | VDD 3.3v for USB |
| 18 | VDD33_IO | P | 3.3V | VDD 3.3v for GPIO |
| 19 | GPIO0 | I/O | | GPIO0 |
| 20 | GPIO2 | I/O | | GPIO2 |
| 21 | GPIO8 | I/O | | GPIO8 |
| 22 | GPIO5 | I/O | | GPIO5 |
| 23 | GPIO4 | I/O | | GPIO4 |
| 24 | GPIO3 | I/O | | GPIO3 |

## 3.3 GPIO Description

Through the software configuration to set flexibly the pull-down & pull-up and input & output

controller of each GPIO.

Each GPIO can also generate interrupts based on the upper and lower edges of the external signal or level to detect the external event triggered.

**Table 3-2 GPIO list .**

| Pin No. | Pin Name | I/O Default Configuration | IO Driving Current | I/O Default Pull-down and pull-up |
|---|---|---|---|---|
| 13 | GPIO9/UART_RXD | input | 5mA | Internal 50K pull-up: 3.3V |
| 19 | GPIO0/JTAG_TCK | input | 5mA | Internal 50K pull-down: 0V |
| 20 | GPIO2/JTAG_TMS | input | 5mA | Internal 50K pull-up: 3.3V |
| 21 | GPIO8 | input | 5mA | Internal 50K pull-down: 0V |
| 22 | GPIO5/JTAG_TDO | Output | 5mA | Internal 50K pull-down: 0V |
| 23 | GPIO4/UART_TXD | Output | 5mA | Internal 50K pull-up: 3.3V |
| 24 | GPIO3/JTAG_TDI | input | 5mA | Internal 50K pull-down: 0V |

# 4. Memory Mapping

## 4.1.1 JTAG Controller

RISC-V CPU realizes JTAG connection by controlling the JTAG controller.

## 4.1.2 On-chip ROM

128KB ROM is used to store ROM code.

| Register Name | Register Address | Size | Description |
|---|---|---|---|
| ROM | 0x0002_0000 ~ 0x0003_FFFF | 128KB | System boot ROM |

## 4.1.3 On-chip RAM

224KB continuous on-chip RAM, RAM0 – RAM3 are used to store code or data.

| Register Name | Register Address | Size | Description |
|---|---|---|---|
| RAM0 | 0x1000_0000 ~ 0x1000_FFFF | 64KB | System on-chip RAM0 |
| RAM1 | 0x1001_0000 ~ 0x1001_FFFF | 64KB | System on-chip RAM1 |
| RAM2 | 0x1002_0000 ~ 0x1002_FFFF | 64KB | System on-chip RAM2 |
| RAM3 | 0x1003_0000 ~ 0x1003_7FFF | 32KB | System on-chip RAM3 |

## 4.1.4 Peri-Dev

The software controls the UART, watchdog, GP timer, GPIO and other peripheral devices by accessing the address register of peripheral devices. APB regis the global control register of the peri device, which is mainly the enable and soft reset control of each device.

| Register Name | Register Address | Size | Description |
|---|---|---|---|
| APB reg | 0x4000_0000 ~ 0x4000_0FFF | 4KB | APB global control register |
| UART | 0x4001_0000 ~ 0x4000_0FFF | 4KB | UATR |
| GPIO | 0x4000_2000 ~ 0x4000_2FFF | 4KB | |
| GP Timer | 0x4000_3000 ~ 0x4000_3FFF | 4KB | |
| Watchdog | 0x4001_4000 ~ 0x40001_4FFF | 4KB | Watchdog |
| PIN_ REG | 0x4000_8000 ~ 0x4000_8FFF | 4KB | IO function selection control |
| ANA_REG | 0x4000_1000 ~ 0x4000_1FFF | 4KB | Analog - Digital interface control |

| Register Name | Register Address | Size | Description |
|---|---|---|---|
| EFUSE | 0x4001_C000 ~ 0x4001_CFFF | 4KB | |
| AHB reg | 0x4001_9000 ~ 0x4001_9FFF | 4KB | AHB reg is the global control register of these co-process-devices, which is mainly the enable and soft reset control of each device |

### 4.1.5 Co-process-Dev

WIFI, USB and other devices through access the high-speed interface and the address register of the coprocessing unit.

| Register Name | Register Address | Size | Description |
|---|---|---|---|
| WIFI | 0x4100_0000 ~ 0x42FF_FFFF | 32MB | |
| USB2.0-CTRL | 0x4800_0000 ~ 0x48FF_FFFF | 16MB | control unit register of usb2.0 |
| USB2.0-PHY | 0x4900_0000 ~ 0x49FF_FFFF | 16MB | PHY unit register of usb2.0 |

# 5. Peripheral Introduction

## 5.1 UART

The WQ9001 supports one channel UART, which can be flexibly used for full-duplex data exchange with external devices and occupies less system resources. The main features areas follows:

- Supports configurable baud rates
- Supports the FIFO size of transmitting and receiving up to 256 Bytes
- Supports parity bits
- Supports for 5/6/7/8 bits data length
- Supports 1/1.5/2/3/4 stop bits
- Supports baud rate up to 3Mbps

The chip default adopts the UART to download the software code, Flash burn, and software upgrade.

## 5.2 General Purpose Timer

The WQ9001 has one sets of GP timer, which can meet various complex timing requirements of the system.

GP timer (General Purpose Timer) generates timing interrupts by counting the internal counter to the specified value. The specified value can be input to modify the configuration by the software. The main features of GP Timer areas follows:

- Supports 32-bit count values
- Supports only upward counting
- Supports to set overflow threshold
- Supports counter latching through GPIO input
- Supports software pause counting and reset
- Contains four independent timers
- Supports two-way timer interconnection to achieve 64-bit counting

## 5.3 Watchdog

The WQ9001 has one WDG (Watch Dog) units, to prevent the system from hanging dead. The features of WDG areas follows:

- Independently set the CPU timeout reset and global timeout reset count
- Independently set the CPU timeout reset and system timeout reset interrupt

- Set the register read and write protection to prevent wrong trigger function
- Flexible set interrupt signal switch and shielding

# 6. Electrical and Thermal Characteristics

## 6.1 Temperature Limit Ratings

**Table 6-1 Temperature Limit Ratings**

| Parameter | Min. | Max. | Units |
|---|---|---|---|
| Storage Temperature | -55 | +125 | °C |
| Ambient Operating Temperature | -40 | +85 | °C |
| Junction Temperature | -40 | +125 | °C |

## 6.2 DC Characteristics

**Table 6-2 Power Supply Characteristics**

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| AVDD33_ADAC_SYN | | 3.0 | 3.3 | 3.6 | V |
| AVDD33_PLLXO | | 3.0 | 3.3 | 3.6 | V |
| AVDD33_BB | | 3.0 | 3.3 | 3.6 | V |
| AVDD33_PA | | 3.0 | 3.3 | 3.6 | V |
| AVDD33_LNA_BIAS | | 3.0 | 3.3 | 3.6 | V |
| VDD33_DLDO | | 3.0 | 3.3 | 3.6 | V |
| VDD33_USB | | 3.0 | 3.3 | 3.6 | V |
| VDD33_IO | | 3.0 | 3.3 | 3.6 | V |
| VDD25_EFUSE | | 2.25 | 2.5 | 2.75 | V |
| VDD11_CORE | | 0.99 | 1.1 | 1.21 | V |

**Table 6-3 Digital IO Pin DC Characteristics**

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage | -- | 0 | 0.9 | V |
| $V_{IH}$ | Input high voltage | 2.0 | 3.3 | 3.6 | V |
| $V_{OL}$ | Output low voltage | 0 | -- | 0.33 | V |
| $V_{OH}$ | Output high voltage | 2.97 | -- | 3.3 | V |

## 6.3 ESD Protection

**Table 6-1 ESD Parameter**

| Test Item | Description | Specification | Value |
|---|---|---|---|
| HBM | All pins except RF_INOUT | JS-001-2017 | 2500V |
| | RF_ INOUT | | 500V |
| CDM | All pins except RF_INOUT | JS-002-2014 | 500V |
| | RF_ INOUT | | 500V |
| Latch up | | JS NO.78E 2016 | 200mA |

# 7. Package Dimensions

The WQ9001 is packaged in a 24-Pin QFN package. The body size is 4 mm by 4 mm. The package drawings and dimensions are provided inFigure 7- 1, Figure 7- 1, Figure 7- 1andTable 7- 1 .

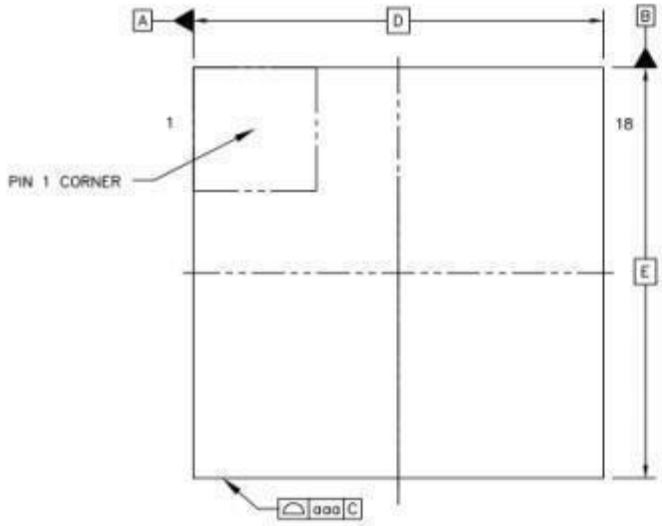


Figure 7-1 To View

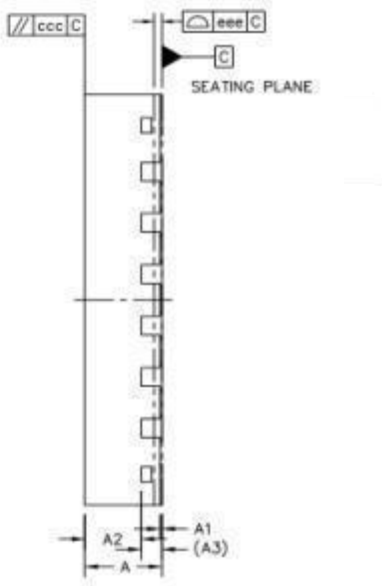


Figure 7-2 Side View

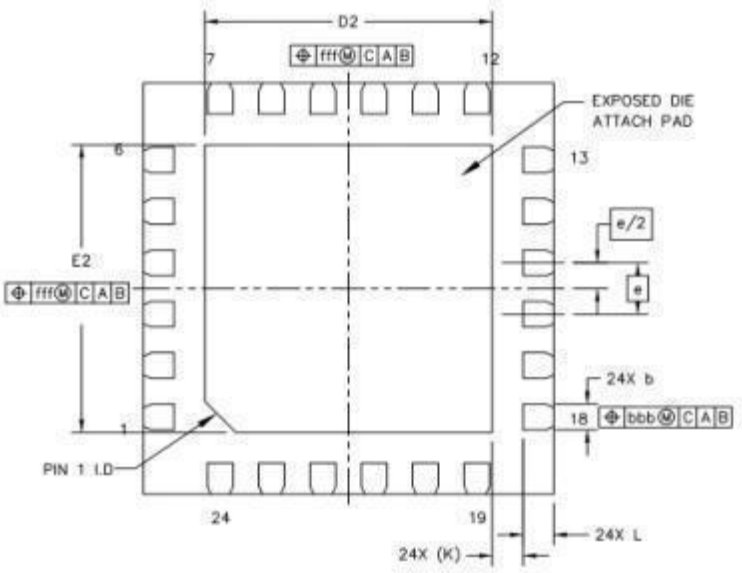


Figure 7-3 Bottom View

Table 7-1 QFN Package Dimensions

| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.7 | 0.75 | 0.8 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.55 | --- |
| L/F THICKNESS | | A3 | | 0.203 REF | |
| LEAD WIDTH | | b | 0.2 | 0.25 | 0.3 |
| BODY SIZE | X | D | | 4 BSC | |
| | Y | E | | 4 BSC | |
| LEAD PITCH | | e | | 0.5 BSC | |
| EP SIZE | X | D2 | 2.7 | 2.8 | 2.9 |
| | Y | E2 | 2.7 | 2.8 | 2.9 |
| LEAD LENGTH | | L | 0.2 | 0.3 | 0.4 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | | 0.3 REF | |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.1 | |
| MOLD FLATNESS | | ccc | | 0.1 | |
| COPLANARITY | | eee | | 0.08 | |
| LEAD OFFSET | | bbb | | 0.1 | |
| EXPOSED PAD OFFSET | | fff | | 0.1 | |

# 8. Device Marking Convention

Figure 8- 1shows the device marking of WQ9001.

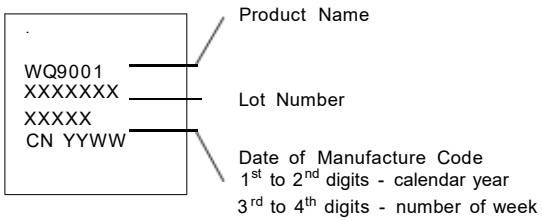


**Figure 8-1 Device Marking of WQ9001**